011607937 **Image available**
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Semiconductor thin film manufacturing method for TFT - involves forming crystalline silicon film by performing dehydrogenation and crystallisation to amorphous silicon film

Patent Assignee: CASIO COMPUTER CO LTD (CASK)
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MANUFACTURE OF SEMICONDUCTOR THIN FILM

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INVENTOR(s): KUDO TOSHIO
WAKAI HARUO
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or Corporation), JP (Japan)
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ABSTRACT

PROBLEM TO BE SOLVED: To enable dehydrogenation and crystallization of a hydrogen-containing amorphous silicon thin film in a short period of time.
SOLUTION: A hydrogen-containing amorphous silicon thin film 25 and a channel protective film forming film 26 made of silicon nitride are continuously deposited on the upper surface of a second gate insulating film 24. Thus, since the amorphous silicon thin film 25 is covered with the channel protective film forming film 26, subsequent dehydrogenation and crystallization processes may be carried out in the atmosphere. By irradiating the amorphous silicon thin film 25 with the light of an excimer lamp in the atmosphere, the amorphous silicon thin film 25 is dehydrogenated. Then, by similarly irradiating the amorphous silicon thin film 25 with an excimer laser in the atmosphere, the amorphous silicon thin film 25 is crystallized, thereby forming a polysilicon thin film 27.

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(71)出願人　000001443
カシオ計算機株式会社
東京都新宿区西新宿２丁目６番１号

(72)発明者　工藤　利雄
東京都八王子市石川町2951番地の５　カシオ計算機株式会社八王子研究所内

(72)発明者　若井　晴夫
東京都八王子市石川町2951番地の５　カシオ計算機株式会社八王子研究所内

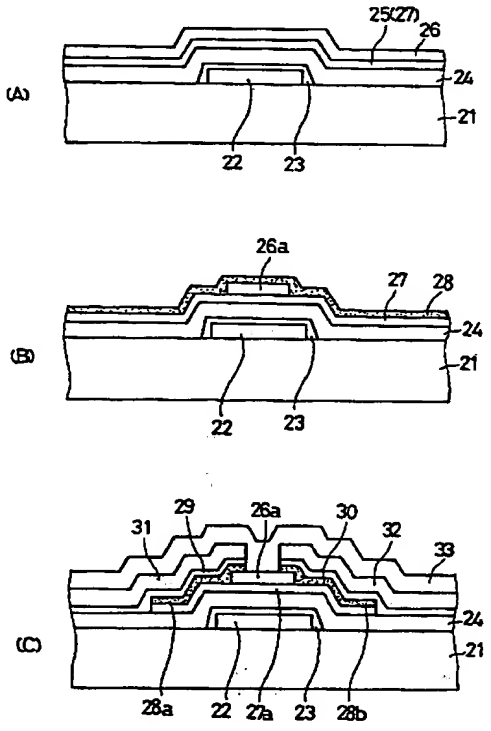
(74)代理人　弁理士　杉村　次郎

(54)【発明の名称】半導体薄膜の製造方法

(57)【要約】

【課題】　水素含有のアモルファスシリコン薄膜の脱水素化及び結晶化を短時間で行うことができるようにする。

【解決手段】　第２ゲート絶縁膜２４の上面に水素含有のアモルファスシリコン薄膜２５および窒化シリコンからなるチャネル保護膜形成用膜２６を連続して成膜する。このように、アモルファスシリコン薄膜２５をチャネル保護膜形成用膜２６で被っているので、後工程の脱水素化工程及び結晶化工程を大気中で行うことが可能となる。そこで、大気中においてエキシマランプの放射光を照射することにより、アモルファスシリコン薄膜２５の脱水素化処理を行い、次いで同じく大気中においてエキシマレーザを照射することにより、アモルファスシリコン薄膜２５を結晶化してポリシリコン薄膜２７を形成する。



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【特許請求の範囲】

【請求項１】　水素含有のアモルファス状の半導体薄膜上に絶縁膜を形成し、常圧雰囲気中において前記半導体薄膜にエキシマ光を照射することにより、前記半導体薄膜を脱水素化するとともに前記半導体薄膜の少なくとも一部を結晶化することを特徴とする半導体薄膜の製造方法。

【請求項２】　請求項１記載の発明において、前記常圧雰囲気は大気であることを特徴とする半導体薄膜の製造方法。

【請求項３】　請求項１または２記載の発明において、前記半導体薄膜の脱水素化はエキシマランプの照射により行い、前記半導体薄膜の結晶化はエキシマレーザの照射により行うことを特徴とする半導体薄膜の製造方法。

【請求項４】　請求項３記載の発明において、前記エキシマランプを照射し、次いで前記エキシマレーザを照射することを特徴とする半導体薄膜の製造方法。

【請求項５】　請求項１～４のいずれかに記載の発明において、前記アモルファス状の半導体薄膜はアモルファスシリコン薄膜であることを特徴とする半導体薄膜の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は半導体薄膜の製造方法に関する。

【０００２】

【従来の技術】半導体薄膜の製造方法には、一例として、成膜したアモルファスシリコン薄膜を結晶化してポリシリコン薄膜とする方法がある。そして、結晶化したポリシリコン薄膜によって薄膜トランジスタを形成することがある。図３は従来のこのようなポリシリコン薄膜トランジスタの製造工程の一例を示し、図４（Ａ）～（Ｄ）はそれぞれ図３に示す製造工程を経て製造されるポリシリコン薄膜トランジスタの各状態における断面図を示したものである。このポリシリコン薄膜トランジスタの製造に際しては、まず図３に示すゲート電極形成工程Ａにおいて、図４（Ａ）に示すように、ガラス基板１の上面の所定の個所にゲート電極２を形成する。次に、図３に示す２層連続成膜工程Ｂにおいて、ゲート電極２を含むガラス基板１の上面全体にゲート絶縁膜３及び水素含有の真性なアモルファスシリコン薄膜４を連続して成膜する。次に、図３に示す脱水素化工程Ｃにおいて、後の工程でエキシマレーザ照射により高エネルギを与えたとき水素が突沸して欠陥が生じるのを避けるために、脱水素化用真空電気炉で熱処理を行うことにより、アモルファスシリコン薄膜４中の水素濃度を低減する。

【０００３】次に、図３に示す結晶化工程Ｄにおいて、真空中においてエキシマレーザを高エネルギ密度で照射することにより、真性なアモルファスシリコン薄膜４を結晶化して真性なポリシリコン薄膜５を形成する。次に、図３に示す不純物注入工程Ｅにおいて、図４（Ｂ）に示すように、ポリシリコン薄膜５のうちチャネル領域５ａとなる領域上に不純物注入マスク６を形成し、ポリシリコン薄膜５のうちチャネル領域５ａとなる領域を除く全領域にリンなどのｎ型不純物を注入する。この後、不純物注入マスク６を剥離する。次に、図３に示す活性化工程Ｆにおいて、エキシマレーザを低エネルギ密度で照射することにより、ｎ型不純物注入領域を活性化する。次に、図３に示すチャネル保護膜形成工程Ｇにおいて、図４（Ｃ）に示すように、ポリシリコン薄膜５のうちチャネル領域５ａとなる領域上にチャネル保護膜７を形成する。

【０００４】次に、図３に示すデバイスエリア形成工程Ｈにおいて、図４（Ｄ）に示すように、ポリシリコン薄膜５のうち不要な部分を除去する。この状態では、ポリシリコン薄膜５の中央部は真性領域からなるチャネル領域５ａとされ、その両側はｎ型不純物注入領域からなるソース領域５ｂ及びドレイン領域５ｃとされている。次に、図３に示すソース・ドレイン電極形成工程Ｉにおいて、チャネル保護膜７の上面両側及びソース領域５ｂ、ドレイン領域５ｃの各上面などにソース電極８及びドレイン電極９を形成する。次に、図３に示すオーバーコート膜成膜工程Ｊにおいて、全上面にオーバーコート膜１０を成膜する。次に、図３に示す水素化工程Ｋにおいて、水素化用電気炉または水素化用プラズマ炉で水素化処理を行うことにより、ポリシリコン薄膜５のダングリングボンドを減少させる。かくして、ボトムゲート型のポリシリコン薄膜トランジスタが製造される。

【発明が解決しようとする課題】

【０００５】ところで、従来のこのようなポリシリコン薄膜トランジスタの製造方法では、図３に示す脱水素化工程Ｃ及び結晶化工程Ｄを行う際、図４（Ａ）に示すように、アモルファスシリコン薄膜４が露出しているので、真空中で行っている。このため、脱水素化工程Ｃ及び結晶化工程Ｄにおける真空引きに時間がかかり、スループットが良くないという問題があった。この発明の課題は、脱水素化工程及び結晶化工程を短時間で行うことができるようにすることである。

【０００６】

【課題を解決するための手段】この発明は、水素含有のアモルファス状の半導体薄膜上に絶縁膜を形成し、常圧雰囲気中において前記半導体薄膜にエキシマ光を照射することにより、前記半導体薄膜を脱水素化するとともに前記半導体薄膜の少なくとも一部を結晶化するようにしたものである。

【０００７】この発明によれば、水素含有のアモルファス状の半導体薄膜上に絶縁膜を形成しているので、半導体薄膜が露出せず、したがって半導体薄膜の脱水素化及び結晶化を常圧雰囲気中において行うことができる。この結果、従来のような真空引きが不要となり、脱水素化

工程及び結晶化工程を短時間で行うことができる。

【０００８】

【発明の実施の形態】図１はこの発明の一実施形態を適用したポリシリコン薄膜トランジスタの製造工程を示し、図２（Ａ）～（Ｃ）はそれぞれ図１に示す製造工程を経て製造されるポリシリコン薄膜トランジスタの各状態における断面図を示したものである。このポリシリコン薄膜トランジスタの製造に際しては、まず図１に示すゲート電極形成工程Ａにおいて、図２（Ａ）に示すように、ガラス基板２１の上面の所定の個所にアルミニウムーチタン合金からなるゲート電極２２を形成する。次に、図１に示す陽極酸化工程Ｂにおいて、陽極酸化処理を行うことにより、ゲート電極２２の表面に酸化アルミニウムからなる第１ゲート絶縁膜２３を形成する。次に、図１に示す３層連続成膜工程Ｃにおいて、第１ゲート絶縁膜２３を含むガラス基板２１の上面全体に、ＰＥ－ＣＶＤにより、窒化シリコンからなる第２ゲート絶縁膜２４、水素含有の真性なアモルファスシリコン薄膜（半導体薄膜）２５及び窒化シリコンからなるチャネル保護膜形成用膜（絶縁膜）２６を連続して成膜する。

【０００９】次に、図１に示す脱水素化・結晶化工程Ｄについて説明するが、この場合、水素含有の真性なアモルファスシリコン薄膜２５上にチャネル保護膜形成用膜２６を成膜しているので、水素含有の真性なアモルファスシリコン薄膜２５が露出せず、したがって常圧雰囲気中例えば大気中において行うことが可能となる。そこで、まず大気中においてエキシマランプの放射光（エキシマ光）を照射することにより、水素含有の真性なアモルファスシリコン薄膜２５の脱水素化処理を行う。この場合、エキシマランプ照射エリアをガラス基板２１を通過させるが、エキシマランプ照射エリアは予備加熱エリアと本加熱エリアとからなっている。予備加熱エリアでは、加熱温度２５０℃以下での連続照射により、本加熱エリアにおいてゲート電極２２及び第１ゲート絶縁膜２３中のアルミニウムにヒロックが発生するのを防止するとともに、ガラス基板２１の熱ストレスを緩和させる。本加熱エリアでは、ゲート電極２２の材料であるアルミニウムーチタン合金の融点以下の高温での連続照射により、水素含有の真性なアモルファスシリコン薄膜２５の脱水素化処理を短時間で行う。

【００１０】次に、同じく大気中においてエキシマレーザ（エキシマ光）を低エネルギ密度で例えば１５０ｍＪ／ｃｍ²程度以下で照射すると、真性なアモルファスシリコン薄膜２５が結晶化して真性なポリシリコン薄膜２７が形成される。この場合、エキシマレーザのエネルギ密度を１５０ｍＪ／ｃｍ²程度以下と低くするのは、特にチャネル保護膜形成用膜２６を形成する窒化シリコン膜に水素が含有されているので、この水素が突沸するのを避けるためである。また、エキシマレーザのエネルギ密度が１５０ｍＪ／ｃｍ²程度以下と低くても、１μｍ程度以下のマイクロクリスタル（結晶化していないものも含む）が形成される。このように、脱水素化工程と結晶化工程とを大気中で連続して行うことができるので、従来のような真空引きが不要となり、脱水素化工程及び結晶化工程を短時間で行うことができ、スループットを良くすることができる。なお、結晶化工程におけるエキシマレーザの照射は、ビームサイズを短い幅を有する細長い帯状とされたレーザビームをビームサイズの幅方向にオーバーラップさせながらスキャン照射することにより行うようにしてもよい。この場合、オーバーラップ量を好ましくは５０％以上、より好ましくは９０～９９％とする。

【００１１】次に、図１に示すチャネル保護膜形成工程Ｅにおいて、図２（Ｂ）に示すように、チャネル保護膜形成用膜２６のうち不要な部分を除去することにより、ポリシリコン薄膜２７上の所定の個所にチャネル保護膜２６ａを形成する。次に、図１に示すｎ型シリコン成膜工程Ｆにおいて、チャネル保護膜２６ａを含むポリシリコン薄膜２７の上面全体にＰＥ－ＣＶＤによりリンなどがドープされたｎ型シリコン膜２８を成膜する。次に、図１に示すデバイスエリア形成工程Ｇにおいて、図２（Ｃ）に示すように、ｎ型シリコン膜２８のうち不要な部分を除去してソース領域２８ａ及びドレイン領域２８ｂを形成するとともに、ポリシリコン薄膜２７のうち不要な部分を除去してチャネル領域２７ａを形成する。すなわち、チャネル保護膜２６ａの上面両側及びその両側におけるチャネル領域２７ａの各上面にソース領域２８ａ及びドレイン領域２８ｂを形成する。この場合、チャネル領域２７ａは真性ポリシリコンからなり、ソース領域２８ａ及びドレイン領域２８ｂはｎ型シリコンからなっている。このように、ソース領域２８ａ及びドレイン領域２８ｂを、成膜したｎ型シリコン膜によって形成しているので、不純物注入工程及び活性化工程が不要となり、したがってこれによっても製造工程を簡略化することができる。なお、ソース領域２８ａ及びドレイン領域２８ｂはｎ型アモルファスシリコンあるいはｎ型ポリシリコンからなるものであってもよい。

【００１２】次に、図１に示すソース・ドレイン電極形成工程Ｈにおいて、ソース領域２８ａ及びドレイン領域２８ｂの各上面などに、クロムからなる第１ソース電極２９及び第１ドレイン電極３０を形成し、続いてその各上面にアルミニウムーチタン合金からなる第２ソース電極３１及び第２ドレイン電極３２を形成する。次に、図１に示すオーバーコート膜成膜工程Ｉにおいて、全上面にオーバーコート膜３３を成膜する。次に、図１に示す水素化工程Ｊにおいて、水素化用電気炉または水素化用プラズマ炉で水素化処理を行うことにより、チャネル領域２７ａ、ソース領域２８ａ及びドレイン領域２８ｂのダングリングボンドを減少させる。かくして、ボトムゲート型のポリシリコン薄膜トランジスタが製造される。

【００１３】ところで、図１に示す製造工程を、従来の同型のつまりボトムゲート型のアモルファスシリコン薄膜トランジスタの製造工程と比較した場合、脱水素化・結晶化工程Ｄが付加されているだけであるので、従来のボトムゲート型のアモルファスシリコン薄膜トランジスタの製造プロセスラインに脱水素化・結晶化工程Ｄのためのエキシマランプ装置及びエキシマレーザ装置を付加すると、従来のボトムゲート型のアモルファスシリコン薄膜トランジスタの製造プロセスラインを若干変更してそのまま使用することにより、この発明のポリシリコン薄膜トランジスタを製造することができることになる。なお、この発明は、ｐ型のポリシリコン薄膜トランジスタにも適用することができる。

【００１４】

【発明の効果】以上説明したように、この発明によれば、アモルファス状の半導体薄膜の脱水素化及び結晶化を常圧雰囲気中において行うことができるので、従来のような真空引きが不要となり、脱水素化工程及び結晶化工程を短時間で行うことができ、スループットを良くすることができる。

【図面の簡単な説明】

【図１】この発明の一実施形態を適用したポリシリコン薄膜トランジスタの製造工程を示す図。

【図２】（Ａ）～（Ｃ）はそれぞれ図１に示す製造工程を経て製造されるポリシリコン薄膜トランジスタの各状態における断面図。

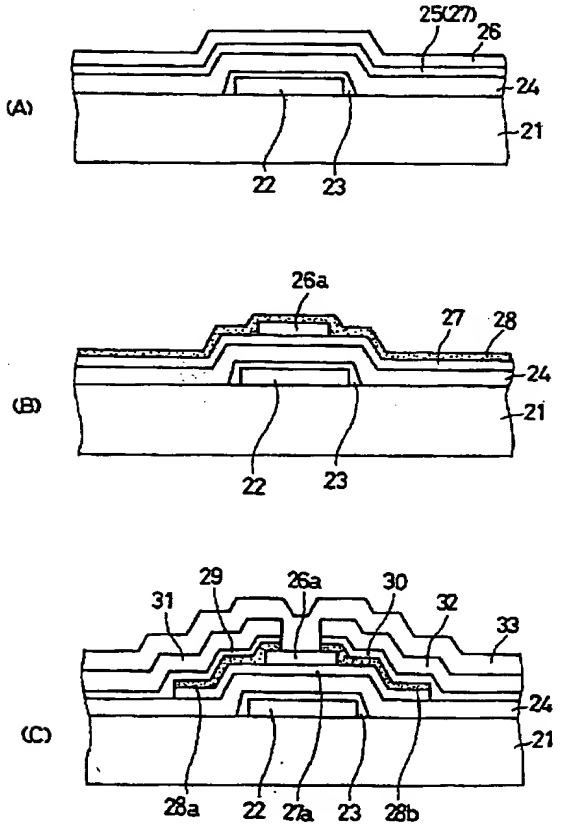
【図３】従来のポリシリコン薄膜トランジスタの製造工程を示す図。

【図４】（Ａ）～（Ｄ）はそれぞれ図３に示す製造工程を経て製造されるポリシリコン薄膜トランジスタの各状態における断面図。

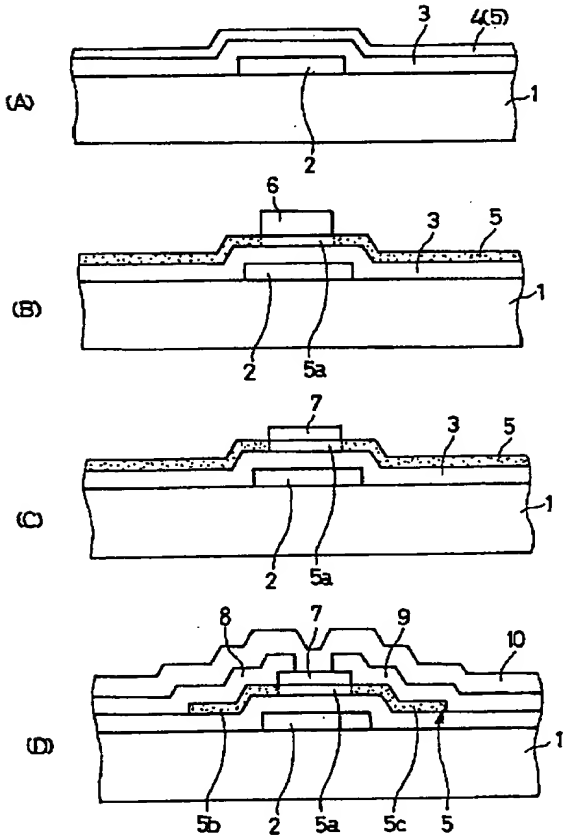
【符号の説明】

２１　ガラス基板
２２　ゲート電極
２３　第１ゲート絶縁膜
２４　第２ゲート絶縁膜
２５　アモルファスシリコン薄膜（半導体薄膜）
２６　チャネル保護膜形成用膜（絶縁膜）
２７　ポリシリコン薄膜

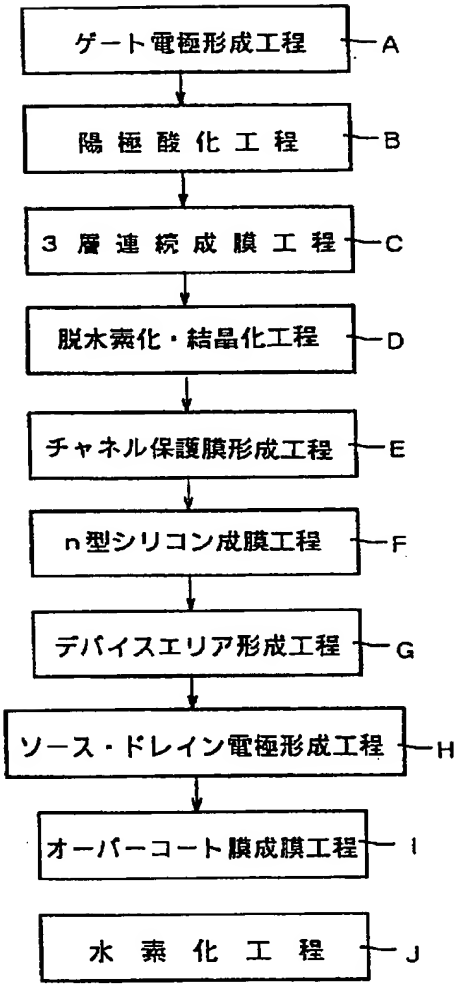
【図２】



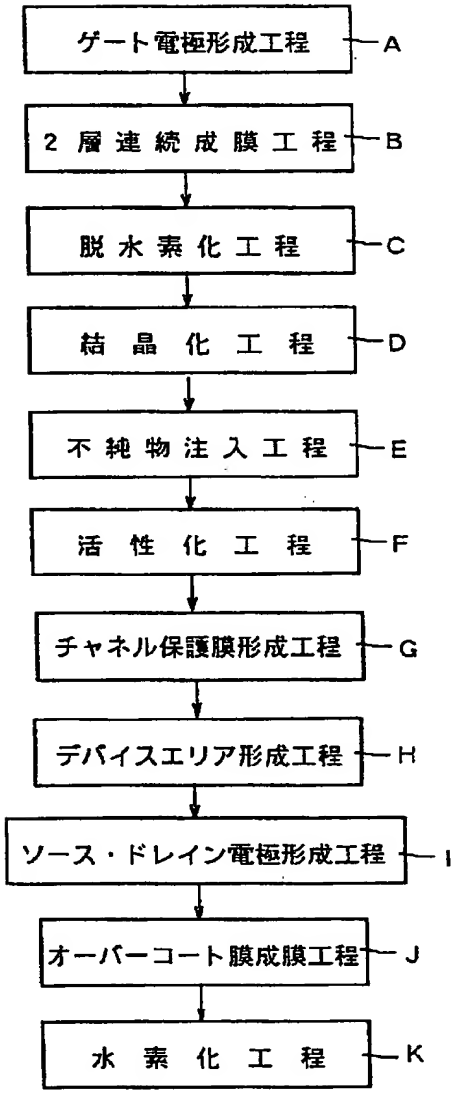
【図４】



【図１】


ゲート電極形成工程
A
陽極酸化工程
B
３層連続成膜工程
C
脱水素化・結晶化工程
D
チャネル保護膜形成工程
E
n型シリコン成膜工程
F
デバイスエリア形成工程
G
ソース・ドレイン電極形成工程
H
オーバーコート膜成膜工程
I
水素化工程
J

【図３】


ゲート電極形成工程
A
２層連続成膜工程
B
脱水素化工程
C
結晶化工程
D
不純物注入工程
E
活性化工程
F
チャネル保護膜形成工程
G
デバイスエリア形成工程
H
ソース・ドレイン電極形成工程
I
オーバーコート膜成膜工程
J
水素化工程
K

PATENT ABSTRACTS OF JAPAN

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(71)Applicant : CASIO COMPUT CO LTD

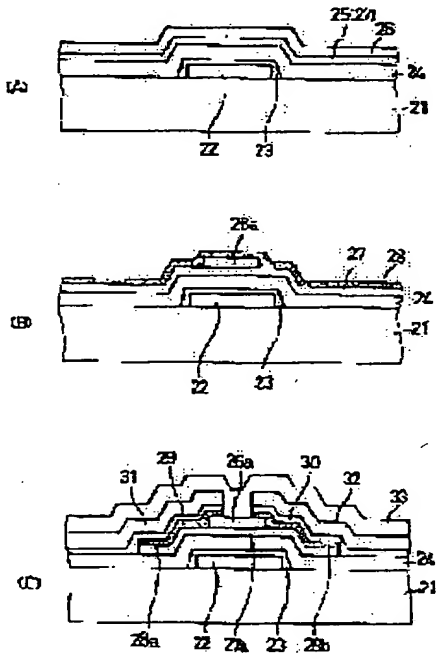
(72)Inventor : KUDO TOSHIO
WAKAI HARUO

(54) MANUFACTURE OF SEMICONDUCTOR THIN FILM

(57)Abstract:

PROBLEM TO BE SOLVED: To enable dehydrogenation and crystallization of a hydrogen-containing amorphous silicon thin film in a short period of time.

SOLUTION: A hydrogen-containing amorphous silicon thin film 25 and a channel protective film forming film 26 made of silicon nitride are continuously deposited on the upper surface of a second gate insulating film 24. Thus, since the amorphous silicon thin film 25 is covered with the channel protective film forming film 26, subsequent dehydrogenation and crystallization processes may be carried out in the atmosphere. By irradiating the amorphous silicon thin film 25 with the light of an excimer lamp in the atmosphere, the amorphous silicon thin film 25 is dehydrogenated. Then, by similarly irradiating the amorphous silicon thin film 25 with an excimer laser in the atmosphere, the amorphous silicon thin film 25 is crystallized, thereby forming a polysilicon thin film 27.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim]
[Claim 1] The manufacture technique of the semiconductor thin film characterized by crystallizing a part of aforementioned semiconductor thin film [at least] while the aforementioned semiconductor thin film is dehydrogenation-ized by forming an insulator layer on the semiconductor thin film of the shape of amorphous [of hydrogen inclusion], and irradiating excimer light into the ordinary-pressure ambient atmosphere at the aforementioned semiconductor thin film.
[Claim 2] It is the manufacture technique of the semiconductor thin film characterized by the aforementioned ordinary-pressure ambient atmosphere being the atmospheric air in invention of claim 1 publication.
[Claim 3] It is the manufacture technique of the semiconductor thin film characterized by for irradiation of an excimer lamp performing dehydrogenation-ization of the aforementioned semiconductor thin film, and performing crystallization of the aforementioned semiconductor thin film by irradiation of an excimer laser in invention the claim 1 or given in two.
[Claim 4] The manufacture technique of the semiconductor thin film characterized by irradiating the aforementioned excimer lamp and subsequently irradiating the aforementioned excimer laser in invention of claim 3 publication.
[Claim 5] It is the manufacture technique of the semiconductor thin film characterized by the semiconductor thin film of the shape of amorphous [aforementioned] being an amorphous silicon thin film in invention given in either of the claims 1-4.

[Translation done.]

DETAILED DESCRIPTION

[Detailed description]
[0001]
[The technical field to which invention belongs] This invention relates to the manufacture technique of a semiconductor thin film.
[0002]
[Prior art] There is the technique of crystallizing the amorphous silicon thin film which ****ed and making it into a polysilicon contest thin film as an example, among the manufacture technique of a semiconductor thin film. And TFT may be formed by the crystallized polysilicon contest thin film. Drawing 3 shows an example of the manufacturing process of such conventional polysilicon contest TFT, and drawing 4 (A) - (D) shows the cross section in each status of the polysilicon contest TFT manufactured through the manufacturing process shown in drawing 3 , respectively. In case of a manufacture of this polysilicon contest TFT, in gate electrode formation process A first shown in drawing 3 , as shown in drawing 4 (A), the gate electrode 2 is formed in the predetermined part of the top of a glass substrate 1. Next, in two-layer continuity **** process B shown in drawing 3 , the gate insulator layer 3 and the genuineness hydrogen inclusion amorphous silicon thin film 4 are continued and ****ed on the whole top of the glass substrate 1 containing the gate electrode 2. Next, in dehydrogenation-ized process C shown in drawing 3 , when a high energy is given by excimer laser irradiation at a next process, in order to avoid that hydrogen bumps and a defect arises, the hydrogen concentration in the amorphous silicon thin film 4 is reduced by heat-treating with the vacuum electric furnace for dehydrogenation-izing.
[0003] Next, in crystallization process D shown in drawing 3 , by irradiating an excimer laser by the high-energy density into a vacuum, the genuineness amorphous silicon thin film 4 is crystallized, and the genuineness polysilicon contest thin film 5 is formed. Next, in impurity injection process E shown in drawing 3 , as shown in drawing 4 (B), the impurity injection mask 6 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5, and n type impurities, such as Lynn, are poured into all the fields except the field which serves as channel field 5a among the polysilicon contest thin films 5. Then, the impurity injection mask 6 is exfoliated. Next, in activation process F shown in drawing 3 , n type impurity injection field is activated by irradiating an excimer laser by the low-energy density. Next, in channel protective coat formation process G shown in drawing 3 , as shown in drawing 4 (C), the channel protective coat 7 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5.
[0004] Next, in device area formation process H shown in drawing 3 , as shown in drawing 4 (D), an unnecessary fraction is removed among the polysilicon contest thin films 5. In this status, the center section of the polysilicon contest thin film 5 is set to channel field 5a which consists of an intrinsic region, and the both sides are set to source field 5b and drain field 5c which consist of an n type impurity injection field. Next, in source drain electrode formation process I shown in drawing 3 , the source electrode 8 and the drain electrode 9 are formed in each top of the top both sides of the channel protective coat 7 and source field 5b, and drain field 5c etc. Next, in overcoat ****** process J shown in

drawing 3 , the overcoat layer 10 is ****ed on all the top. Next, in hydrogenation process K shown in drawing 3 , the dangling bond of the polysilicon contest thin film 5 is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.

[Object of the Invention]

[0005] By the way, by the manufacture technique of such conventional polysilicon contest TFT, since the amorphous silicon thin film 4 is exposed as shown in drawing 4 (A) in case dehydrogenation-ized process C and crystallization process D which are shown in drawing 3 are performed, it is carrying out in the vacuum. For this reason, the vacuum length in dehydrogenation-ized process C and crystallization process D took time, and there was a problem that a throughput was not good. The technical probrem of this invention is enabling it to perform a dehydrogenation-ized process and a crystallization process for a short time.

[0006]

[The means for solving a technical problem] This invention forms an insulator layer on the semiconductor thin film of the shape of amorphous [of hydrogen inclusion], and by irradiating excimer light into the ordinary-pressure ambient atmosphere at the aforementioned semiconductor thin film, it crystallizes a part of aforementioned semiconductor thin film [at least] while it dehydrogenation-izes the aforementioned semiconductor thin film.

[0007] According to this invention, since the insulator layer is formed on the semiconductor thin film of the shape of amorphous [of hydrogen inclusion], a semiconductor thin film cannot be exposed, therefore dehydrogenation-izing and crystallization of a semiconductor thin film can be performed into the ordinary-pressure ambient atmosphere. Consequently, vacuum length like before becomes unnecessary and a dehydrogenation-ized process and a crystallization process can be performed for a short time.

[0008]

[Gestalt of implementation of invention] Drawing 1 shows the manufacturing process of the polysilicon contest TFT which applied the 1 enforcement gestalt of this invention, and drawing 2 (A) - (C) shows the cross section in each status of the polysilicon contest TFT manufactured through the manufacturing process shown in drawing 1 , respectively. In case of a manufacture of this polysilicon contest TFT, as gate electrode formation process A first shown in drawing 1 is shown in drawing 2 (A), the gate electrode 22 which consists of an aluminum-titanium alloy is formed in the predetermined part of the top of a glass substrate 21. Next, in anodic oxidation process B shown in drawing 1 , the 1st gate insulator layer 23 which consists of an aluminum oxide is formed in the front face of the gate electrode 22 by performing an anodizing. Next, in three layer continuity **** process C shown in drawing 1 , the layer (insulator layer) for channel protective coat formation 26 which consists of the 2nd gate insulator layer 24, the genuineness hydrogen inclusion amorphous silicon thin film (semiconductor thin film) 25, and silicon nitride which consist of a silicon nitride is continuously ****ed by PE-CVD on the whole top of the glass substrate 21 containing the 1st gate insulator layer 23.

[0009] Next, although dehydrogenation-izing and crystallization process D shown in drawing 1 are explained, since the layer for channel protective coat formation 26 is ****ed on the genuineness hydrogen inclusion amorphous silicon thin film 25 in this case, it is enabled for the genuineness hydrogen inclusion amorphous silicon thin film 25 not to be exposed, therefore to carry out into the ordinary-pressure ambient atmosphere, for example, the atmospheric air. Then, dehydrogenation-ized processing of the genuineness hydrogen inclusion amorphous silicon thin film 25 is performed by irradiating the synchrotron orbital radiation (excimer light) of an excimer lamp into the atmospheric air first. In this case, although a glass substrate 21 is passed, the excimer lamp irradiation area consists the excimer lamp irradiation area of a preheating area and this heating area. While it prevents that reach gate electrode 22 in this heating area, and a hillock occurs to the aluminum in the 1st gate insulator layer 23 by the continuous irradiation with a heating temperature of 250 degrees C or less, the heat stress of a glass substrate 21 is made to ease in a preheating area. In this heating area, the continuous irradiation in the elevated temperature below the melting point of the aluminum-titanium alloy which is the material

of the gate electrode 22 performs dehydrogenation-ized processing of the genuineness hydrogen inclusion amorphous silicon thin film 25 for a short time.
[0010] Next, if it is 2 or less-about 150mJ/cm and an excimer laser (excimer light) is similarly irradiated by the low-energy density into the atmospheric air, the genuineness amorphous silicon thin film 25 will crystallize, and the genuineness polysilicon contest thin film 27 will be formed. In this case, since hydrogen contains in the silicon nitride film which forms the layer for channel protective coat formation 26, it is for avoiding that this hydrogen bumps especially to make the energy density of an excimer laser low with 2 or less-about 150mJ/cm. Moreover, even if the energy density of an excimer laser is as low as 2 or less-about 150mJ/cm, micro crystal (what is not being crystallized is included) about 1 micrometer or less is formed. Thus, since a dehydrogenation-ized process and a crystallization process can be continuously performed in the atmospheric air, vacuum length like before can become unnecessary, can perform a dehydrogenation-ized process and a crystallization process for a short time, and can improve a throughput. In addition, you may be made to perform irradiation of the excimer laser in a crystallization process by carrying out scanning irradiation, making the long and slender laser beam which has short width of face for a beam size and which was made beltlike overlap crosswise [of a beam size]. In this case, the amount of overlap is more preferably made into 90 - 99% 50% or more.
[0011] Next, in channel protective coat formation process E shown in drawing 1 , as shown in drawing 2 (B), channel protective coat 26a is formed in the predetermined part on the polysilicon contest thin film 27 by removing an unnecessary fraction among the layers for channel protective coat formation 26. Next, in n type silicon **** process F shown in drawing 1 , n type silicon layer 28 by which Lynn etc. was doped by the whole top of the polysilicon contest thin film 27 containing channel protective coat 26a by PE-CVD is ****ed. Next, in device area formation process G shown in drawing 1 , as shown in drawing 2 (C), while an unnecessary fraction is removed among n type silicon layers 28 and source field 28a and drain field 28b are formed, an unnecessary fraction is removed among the polysilicon contest thin films 27, and channel field 27a is formed. That is, source field 28a and drain field 28b are formed in the top both sides of channel protective coat 26a, and each top of channel field 27a in the both sides. In this case, channel field 27a consists of contest intrinsic polysilicon, and source field 28a and drain field 28b consist of n type silicon. Thus, since source field 28a and drain field 28b are formed with n type silicon layer which ****ed, an impurity injection process and an activation process become unnecessary, therefore a manufacturing process can be simplified also by this. In addition, source field 28a and drain field 28b may consist of an n type amorphous silicon or contest n type polysilicon.
[0012] the [next, / the 1st source electrode 29 which becomes each top of source field 28a and drain field 28b etc. from chromium in source drain electrode formation process H shown in drawing 1 , and] -- the [the 2nd source electrode 31 which forms 1 drain electrode 30, and becomes each of that top from an aluminum-titanium alloy continuously, and] -- 2 drain electrode 32 is formed Next, in overcoat ****** process I shown in drawing 1 , the overcoat layer 33 is ****ed on all the top. Next, in hydrogenation process J shown in drawing 1 , the dangling bond of channel field 27a, source field 28a, and drain field 28b is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.
[0013] by the way, when [with the former of the same type] it is got blocked and it compares with the manufacturing process of bottom gate type amorphous silicon TFT, the manufacturing process shown in drawing 1 [only being added to dehydrogenation-izing and crystallization process D, and] If the excimer lamp equipment and excimer laser equipment for dehydrogenation-izing and crystallization process D are added to the manufacture process line of conventional bottom gate type amorphous silicon TFT The polysilicon contest TFT of this invention can be manufactured by changing the manufacture process line of conventional bottom gate type amorphous silicon TFT a little, and using it as it is. In addition, this invention is applicable also to p type polysilicon contest TFT.
[0014]
[Effect of the invention] Since dehydrogenation-izing and crystallization of the shape of amorphous of a semiconductor thin film can be performed into the ordinary-pressure ambient atmosphere according to

this invention as explained above, vacuum length like before can become unnecessary, can perform a dehydrogenation-ized process and a crystallization process for a short time, and can improve a throughput.

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TECHNICAL FIELD

[The technical field to which invention belongs] This invention relates to the manufacture technique of a semiconductor thin film.

[Translation done.]

PRIOR ART

[Prior art] There is the technique of crystallizing the amorphous silicon thin film which ****ed and making it into a polysilicon contest thin film as an example, among the manufacture technique of a semiconductor thin film. And TFT may be formed by the crystallized polysilicon contest thin film. Drawing 3 shows an example of the manufacturing process of such conventional polysilicon contest TFT, and drawing 4 (A) - (D) shows the cross section in each status of the polysilicon contest TFT manufactured through the manufacturing process shown in drawing 3 , respectively. In case of a manufacture of this polysilicon contest TFT, in gate electrode formation process A first shown in drawing 3 , as shown in drawing 4 (A), the gate electrode 2 is formed in the predetermined part of the top of a glass substrate 1. Next, in two-layer continuity **** process B shown in drawing 3 , the gate insulator layer 3 and the genuineness hydrogen inclusion amorphous silicon thin film 4 are continued and ****ed on the whole top of the glass substrate 1 containing the gate electrode 2. Next, in dehydrogenation-ized process C shown in drawing 3 , when a high energy is given by excimer laser irradiation at a next process, in order to avoid that hydrogen bumps and a defect arises, the hydrogen concentration in the amorphous silicon thin film 4 is reduced by heat-treating with the vacuum electric furnace for dehydrogenation-izing.

[0003] Next, in crystallization process D shown in drawing 3 , by irradiating an excimer laser by the high-energy density into a vacuum, the genuineness amorphous silicon thin film 4 is crystallized, and the genuineness polysilicon contest thin film 5 is formed. Next, in impurity injection process E shown in drawing 3 , as shown in drawing 4 (B), the impurity injection mask 6 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5, and n type impurities, such as Lynn, are poured into all the fields except the field which serves as channel field 5a among the polysilicon contest thin films 5. Then, the impurity injection mask 6 is exfoliated. Next, in activation process F shown in drawing 3 , n type impurity injection field is activated by irradiating an excimer laser by the low-energy density. Next, in channel protective coat formation process G shown in drawing 3 , as shown in drawing 4 (C), the channel protective coat 7 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5.

[0004] Next, in device area formation process H shown in drawing 3 , as shown in drawing 4 (D), an unnecessary fraction is removed among the polysilicon contest thin films 5. In this status, the center section of the polysilicon contest thin film 5 is set to channel field 5a which consists of an intrinsic region, and the both sides are set to source field 5b and drain field 5c which consist of an n type impurity injection field. Next, in source drain electrode formation process I shown in drawing 3 , the source electrode 8 and the drain electrode 9 are formed in each top of the top both sides of the channel protective coat 7 and source field 5b, and drain field 5c etc. Next, in overcoat ****** process J shown in drawing 3 , the overcoat layer 10 is ****ed on all the top. Next, in hydrogenation process K shown in drawing 3 , the dangling bond of the polysilicon contest thin film 5 is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.

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EFFECT OF THE INVENTION

[Effect of the invention] Since dehydrogenation-izing and crystallization of the shape of amorphous of a semiconductor thin film can be performed into the ordinary-pressure ambient atmosphere according to this invention as explained above, vacuum length like before can become unnecessary, can perform a dehydrogenation-ized process and a crystallization process for a short time, and can improve a throughput.

[Translation done.]